FIG 1

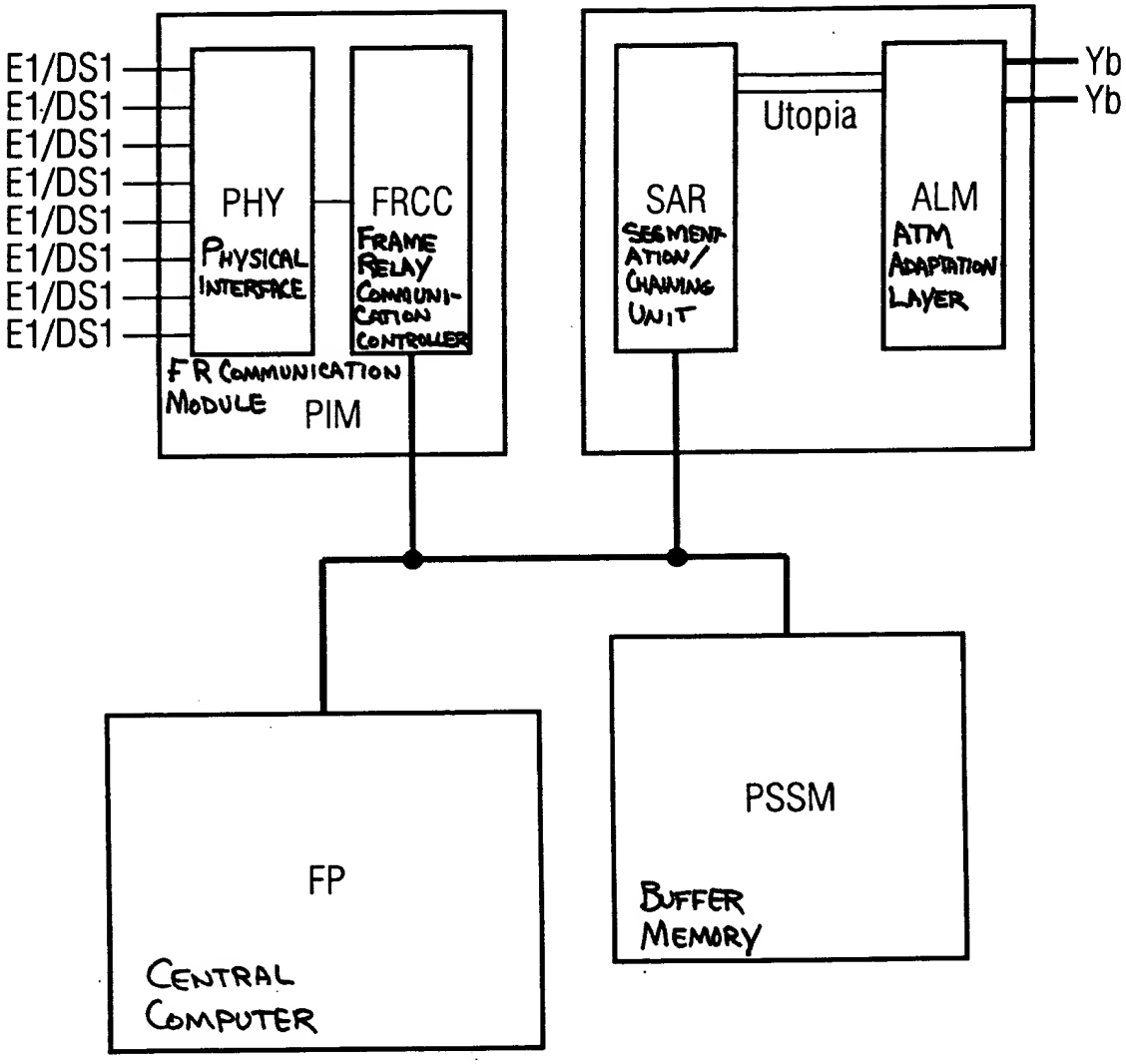

E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
PHY
PHYSICAL INTERFACE
FRCC
FRAME RELAY COMMUNICATION CONTROLLER
FR COMMUNICATION MODULE
PIM
SAR
SEGMENTATION/CHANNING UNIT
Utopia
ALM
ATM ADAPTATION LAYER
Yb
Yb
FP
CENTRAL COMPUTER
PSSM
BUFFER MEMORY

FIG 2

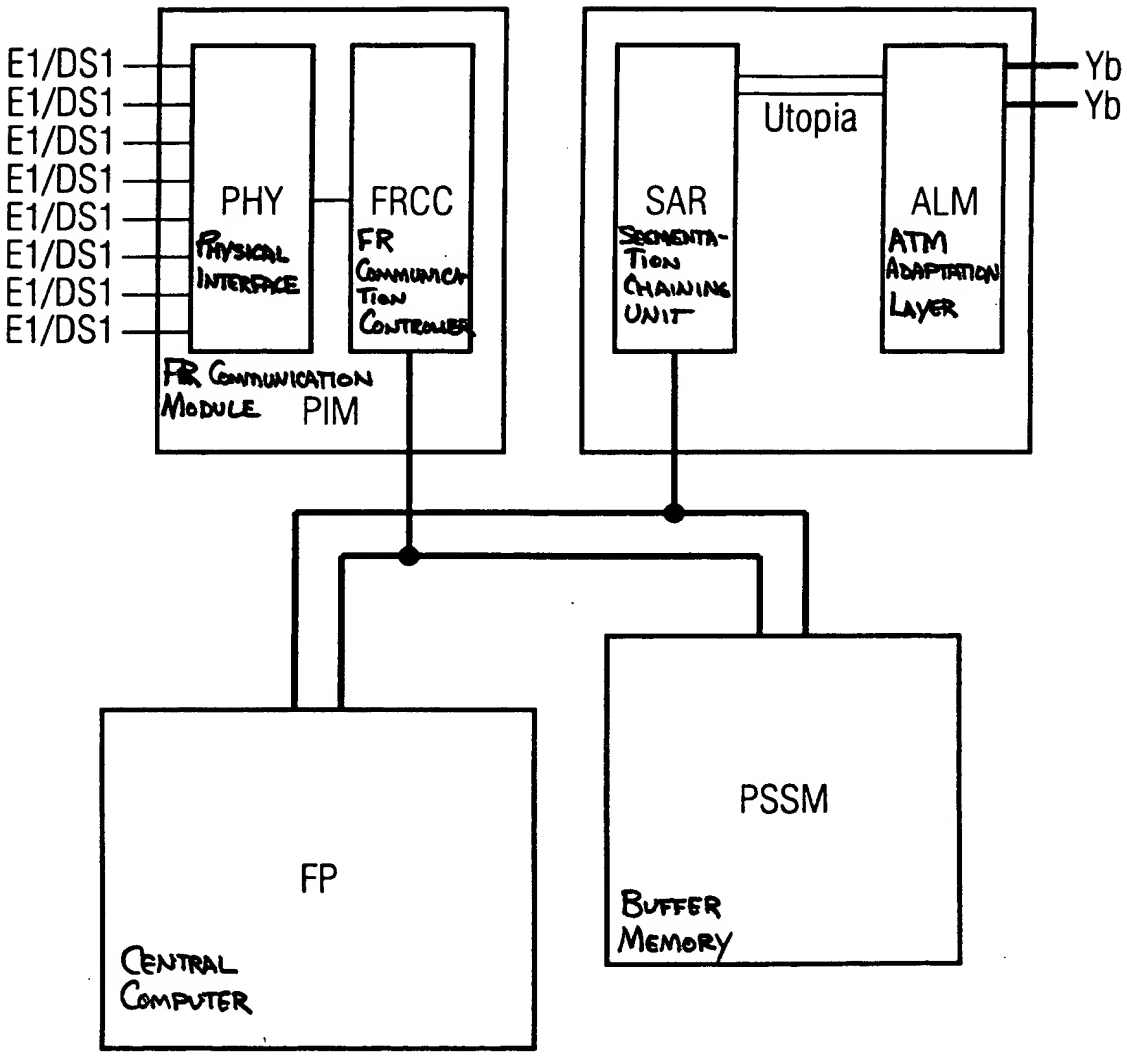

E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
PHY
PHYSICAL INTERFACE
FRCC
FR COMMUNICATION CONTROLLER
FR COMMUNICATION MODULE
PIM
SAR
SEGMENTATION CHAINING UNIT
Utopia
ALM
ATM ADAPTATION LAYER
Yb
Yb
FP
CENTRAL COMPUTER
PSSM
BUFFER MEMORY

FIG 3

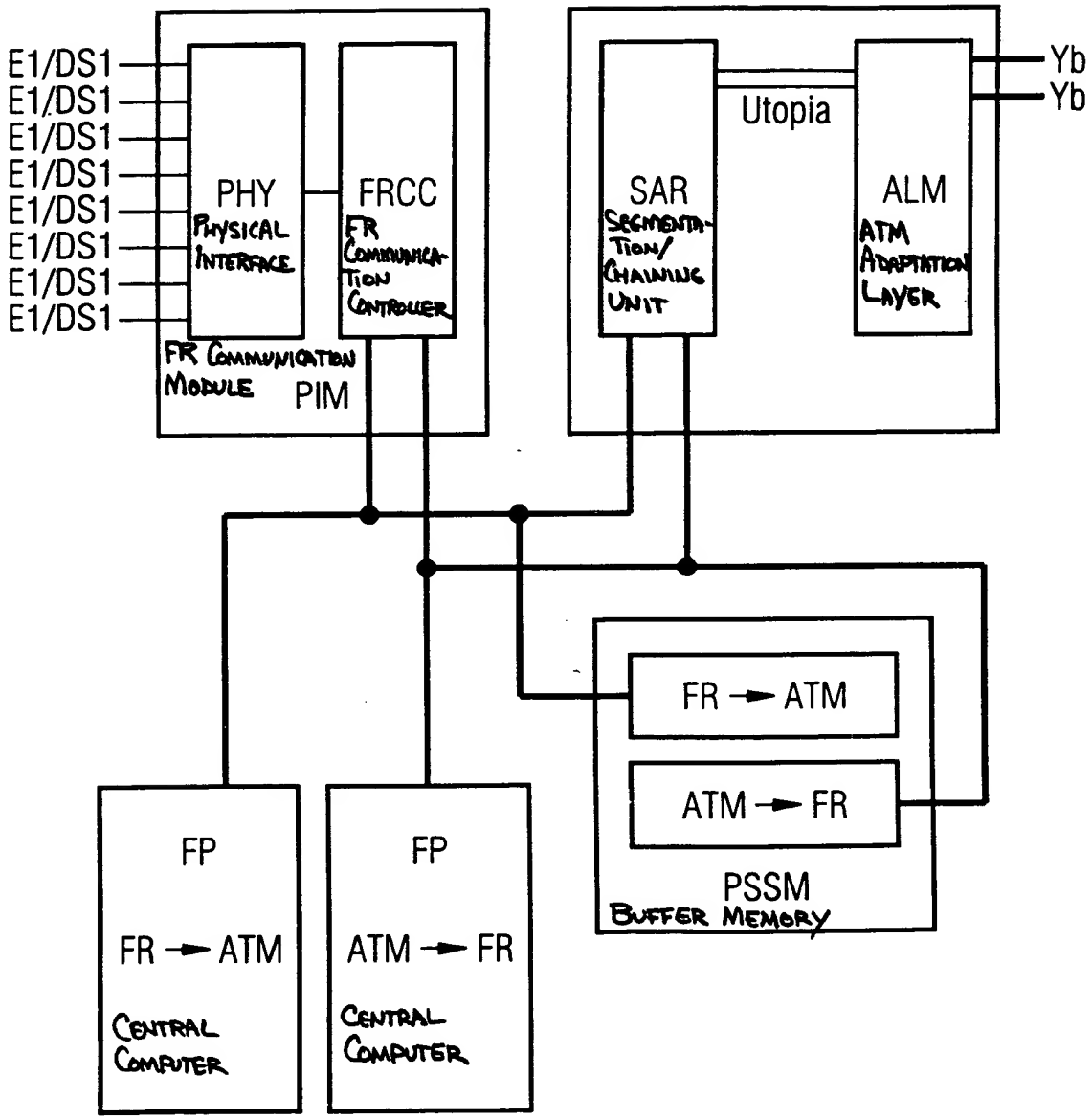

E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
PHY
PHYSICAL INTERFACE
FRCC
FR COMMUNICATION CONTROLLER
FR COMMUNICATION MODULE
PIM
SAR
SEGMENTATION/ CHAINING UNIT
Utopia
ALM
ATM ADAPTATION LAYER
Yb
Yb
FR → ATM
ATM → FR
PSSM
BUFFER MEMORY
FP
FR → ATM
CENTRAL COMPUTER
FP
ATM → FR
CENTRAL COMPUTER

FIG 4

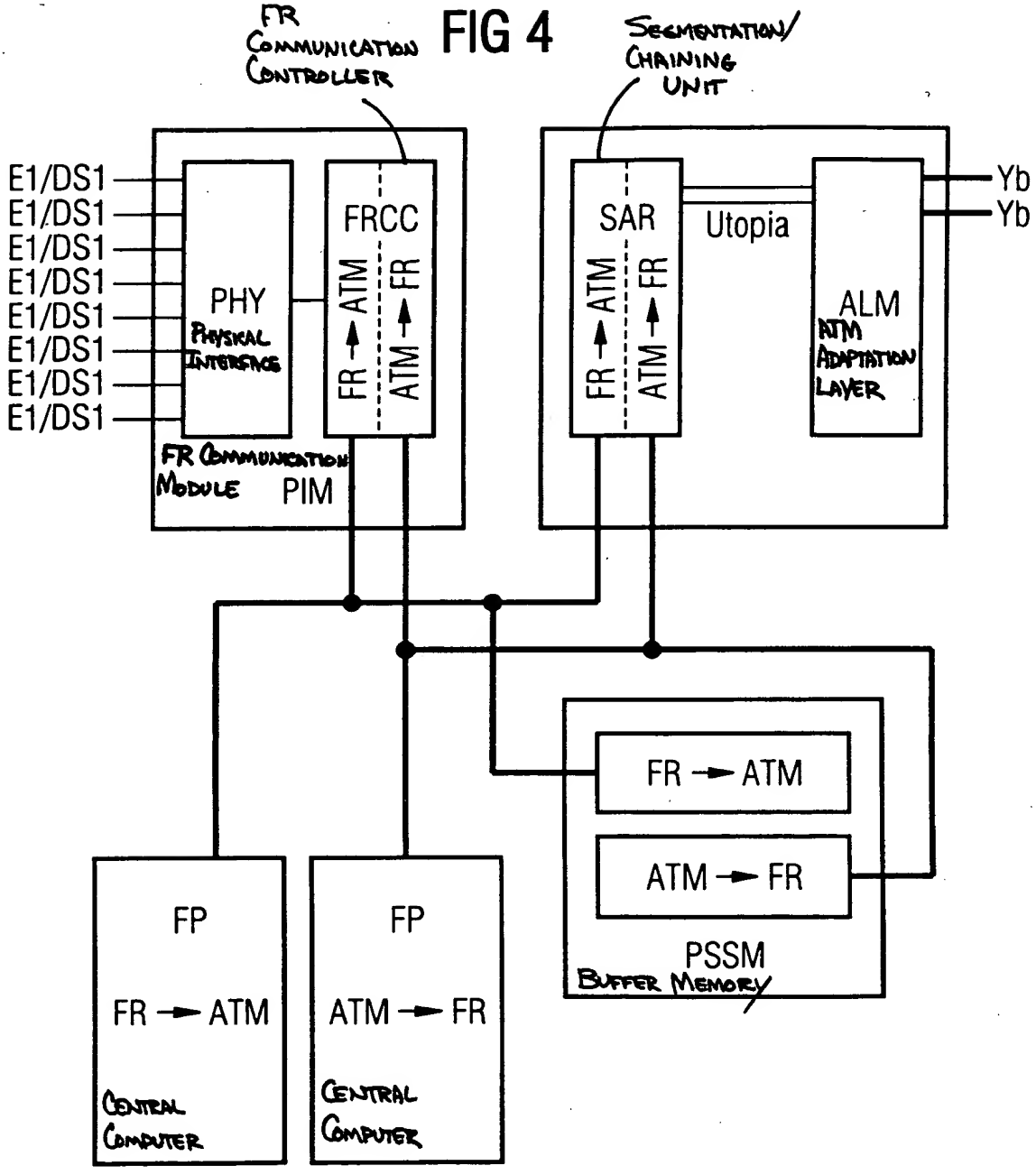
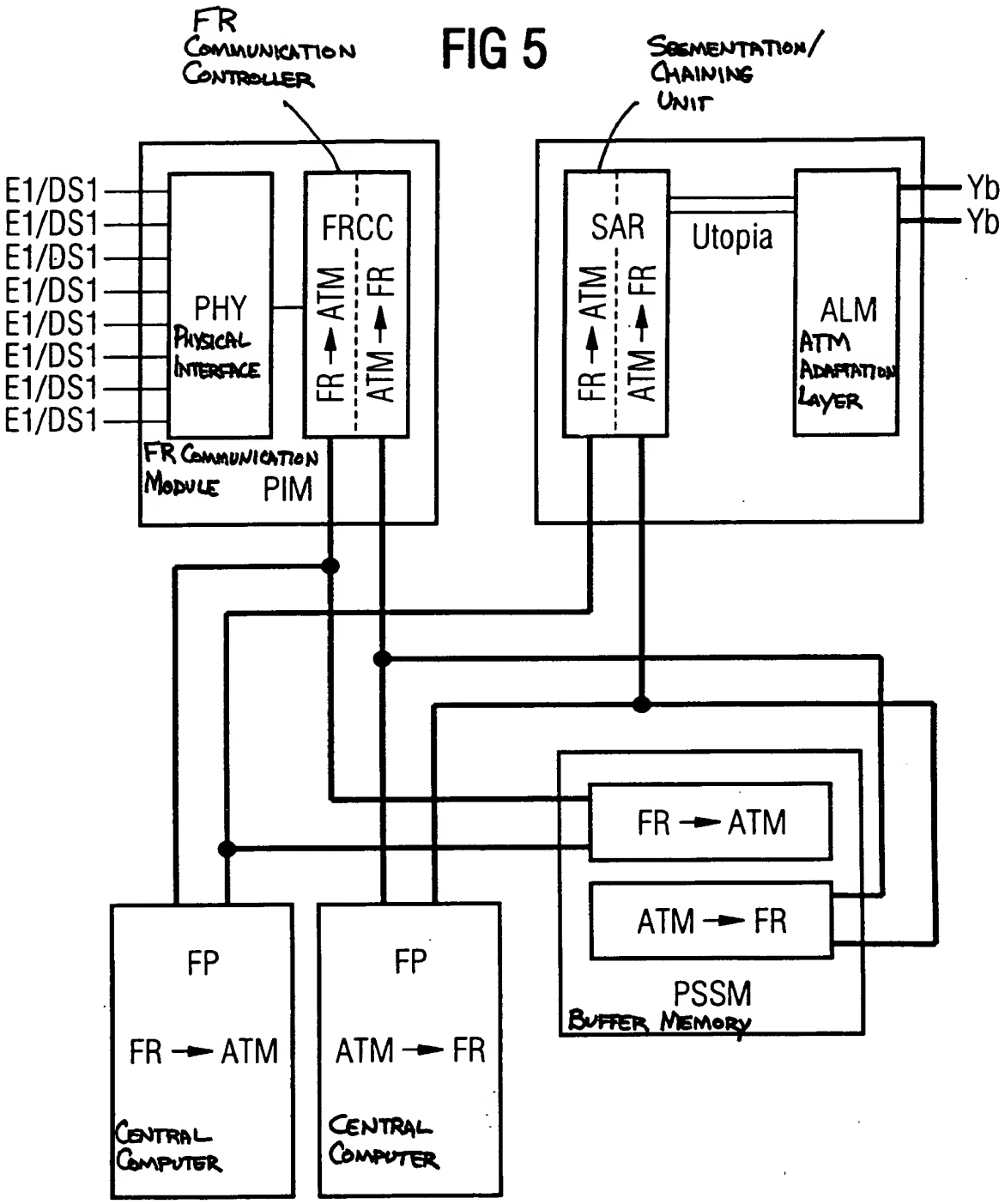

FR COMMUNICATION CONTROLLER
SEGMENTATION/ CHAINING UNIT
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
PHY
PHYSICAL INTERFACE
FRCC
FR → ATM
ATM → FR
FR COMMUNICATION MODULE PIM
SAR
FR → ATM
ATM → FR
Utopia
ALM
ATM ADAPTATION LAYER
Yb
Yb
FR → ATM
ATM → FR
PSSM
BUFFER MEMORY
FP
FR → ATM
CENTRAL COMPUTER
FP
ATM → FR
CENTRAL COMPUTER

FIG 5


FR COMMUNICATION CONTROLLER
SEGMENTATION/ CHAINING UNIT
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
E1/DS1
PHY PHYSICAL INTERFACE
FRCC
FR → ATM
ATM → FR
FR COMMUNICATION MODULE PIM
SAR
FR → ATM
ATM → FR
Utopia
ALM ATM ADAPTATION LAYER
Yb
Yb
FR → ATM
ATM → FR
PSSM BUFFER MEMORY
FP
FR → ATM
CENTRAL COMPUTER
FP
ATM → FR
CENTRAL COMPUTER